Electrical Properties of $Pb_{1-x} Ca_x TiO_3$ (x=0.12mol) Film

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Abstract

Calcium doped lead titanate (PCT) powder film will be firstly prepared by Sol-gel processing. It will be obtained on p- type Si (100) substrate of different process temperatures. The spin coating techniques will be used in this study. Scanning Electron Microscopy (SEM) investigation will be carried out to identify the surface morphology and microstructural properties of fabricated film. Film thickness can be obtained by cross-sectional SEM microphotograph. The electrical property, current (I)-voltage (V) variation can be observed from this research. From I-V curve, threshold voltage (V_{TH}), low voltage resistance (LVR) and maximum current (I_{max}) can be measured. From ln I-V curve, linear relation ideality factor and zero - bias barrier height will be investigated at 500˚C, 550˚C, 600˚C,650˚C and 700˚C respectively.

Keywords: surface morphology, I-V characteristics, threshold voltage, low voltage resistance, maximum current, ideality factor, zero-bias barrier height

Introduction

The promising properties of ferroelectric material for non-volatile memory application has increased activities on ferroelectric thin films all over the world. Considerable attention is focused on ferroelectric devices, particularly non-volatile memory devices.

Ferroelectric materials can be used in different ways in memory designs. Considerable attention has been recently paid to ferroelectric random access memories (FeRAMs), which are non-volatile memory devices using ferroelectric thin films. Since they retain information when power is interrupted, they will constitute as the important computer components. $Pb_{1-x} Ca_x TiO_3$(abbreviated to PCT) have been promising candidates for ferroelectric memory devices: these materials exhibit relatively small dielectric constants. Among the various ferroelectrics; $PbTiO_3$ films were paid less attention, due to high coercive field, large c/a of the parent $PbTiO_3$ unit cell and facilitates ferroelectric switching [1~5].The purpose of this paper is to investigate the sample preparation, surface morphology , thickness and I-V characteristics of lead-based titanate film formed on p-Si (100) substrate. Microstructural and electrical properties of the PCT film have been performed.

Experimental

PbO and TiO_2 were used as starting materials. The purity of materials was 99.9%. Firstly PbO and TiO_2 were mixed with according to the stoichiometric composition. CaO was added to this mixture. Then the mixture powder was grounded by agate motor for 2hr to obtain homogeneous and uniform grain size. And then a beaker was washed with acetone and dried at room temperature. The mixture powder was placed in that beaker appropriate amount of acetone was added and stirred thoroughly till the powder became homogeneous. After the previous cases, the mixture powder was grounded by electric motor for 2hr and annealed at 650°C for 1hr in O_2-ambient to be crystalline. The crystalline powders were dissolved in 2-methoxyethanol solvent. The mixture solution was acidified with HCl. The solution were stirred and refluxed up to 100°C for 2 hr and cooled to room temperature. The p-Si(100) substrates were cleaned by standard semiconductor cleaning method. The PCT precursor solutions were spin-coated onto p-Si (100) substrates to obtain films with Ca contents of

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x= 12mol% were designed as PCT 12 memory devices and annealed at 500°C, 550°C, 600°C, 650°C and 700°C for 1 hr.

Scanning Electron Microscopy Measurement System

The Scanning Electron Microscope (SEM) is a microscope that uses electrons rather than light to form an image. There are many advantages to using the SEM instead of a light microscope. The SEM has a large depth of field, which allows a large amount of the sample to be in focus at one time. The SEM also produces images of high resolution, which means that closely spaced features can be examined at a high magnification. (Fig. 1) represented scanning electron microscope.

SEM is one of the most versatile instruments available for the examination and analysis of the microstructure characteristics of a solid. The most important reason for using the SEM is the high resolution that can be obtained when bulk sample are examined. Resolution on the other of 2 to 5 nm is now usually quoted for commercial instruments. Instruments with resolutions better than 1 nm are also available.

Another important feature of SEM is the three-dimensional appearance of the image. This is a direct result of the large depth of field, as well as the shadow-relief effects of the secondary and backscattered electron contrast. The greater depth of field of the SEM provides more information about the specimen. Most SEM micrograph has been produced with the magnification below 8000 x 8000 (diameters). At this magnification the SEM is operating well within its resolution capacities.

The specimen, which is often coated with a metal such as gold prior to the measurement to achieve better contrast, is placed in a vacuum chamber. A focused electron beam is then scanned across its surface in synchronism in with the spot of a display cathode ray tube. A detector monitors the intensity of a chosen secondary signal from the specimen (usually, secondary electrons are use used), and the brightness of the spot on the display is determined by an amplified version of the detected signal. If the intensity of the emitted secondary signal changes across the specimen, then contrast will be seen in the image on the cathode ray tube. The resulting image reflects the surface topography of the specimen and can be readily interpreted because it contains light and shade in much the same way as everyday which are familiar to our eye.

Figure (1). Scanning Electron Microscope

Current-voltage Characteristics

The Schottky diodes have been made on a number of semiconductors: most of the devices follow the I-V relation of the form

$$I=I_s \exp\left[\frac{qV}{\eta\, kT}\right] \qquad (1)$$

where η is called the ideality factor, I_s is the forward saturation current, V_{TH} is the threshold voltage, 0.02586V for room temperature and V is the bias voltage drop across the semiconductor surface depletion layer.

It is seen that in the forward direction, the current I rises exponentially with the voltage, whereas in the reverse direction, it saturates to a value I_s. In an current–voltage experiment, the junction current is measured as a function of the applied bias voltage. From a plot of the logarithmic of the forward bias current, the saturation current, I_s and the ideality factor, η can be determined. According to the thermionic emission theory, the diode saturation current is related to the Schotty barrier height by the following equation.

$$I_s=AR^*T2 \exp\left[-\frac{q\phi bo}{kT}\right] \qquad (2)$$

where R^* is the Richardson's constant for the semiconductor, A is the electrode area and T is the room temperature, ϕ_{bo} is the zero-biased barrier height and k is the Boltzmann constant. Zero-biased barrier height, ϕ_{bo} can be obtained from equation (2) . The copper electrode, multimeter and other required specimen were used to measure the I-V characteristics of PCT films. The circuit arrangement for current-voltage characteristics measurement in laboratory was shown in (Fig. 2)

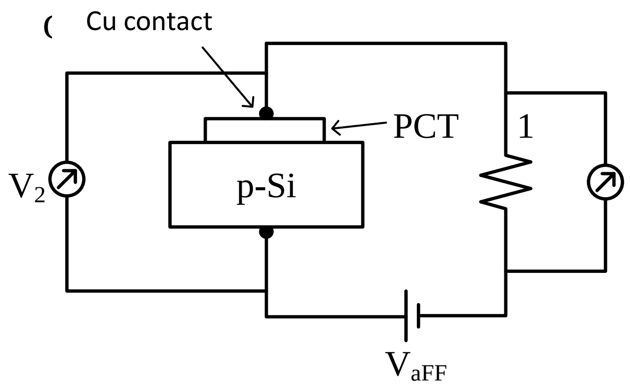

Figure (2). Circuit arrangement for current-voltage (I-V) measurement

Result and Discussion

Scanning Electron Microscopy (SEM) investigation was carried out to identify the surface morphology and microstructural properties of fabricated film. The observed SEM images were shown in (Figs. 3.a - 3.e). All SEM images were found to be crack-free. Uniform grain distribution was observed in all images. They looked fairly dense in microstructure. The grain orientations of all films were toward the left, except the films at 550°C and 700°C. The surface morphology of SEM micrographs were seen to be smooth, except in those of the films at 600°C and 650°C. Thus, all SEM images were almost the same in microstructure. Microstructural properties of PCT films were listed in table (1).

Table(1). Microstructural properties of PCT film by Scanning Electron Microscope (SEM) Analysis

Temperature	**Microstructural Properties**				
500°C	Left	Uniform	Fairly dense	Crack free	Smooth
550°C	Right	Uniform	Fairly dense	Crack free	Smooth
600°C	Left	Uniform	Fairly dense	Crack free	Rough
650°C	Left	Uniform	Fairly dense	Crack free	Rough
700°C	Right	Uniform	Fairly dense	Crack free	Smooth

The grain size were calculated to be 0.36µm, 0.35µm, 0.35µm, 0.32µm and 0.37µm, respectively. (Fig. 4) showed the grain size versus process temperature of Ca modified $PbTiO_3$. The thickness of fabricated film could be obtained from cross sectional SEM image. They were described up (Figs.5.a - 5.e). The film thickness were 24.5µm, 27.0µm, 25.3µ, 28.6µm and 25.3µm for respectively films. Figure (6) represented the variation of thicknesses according to the respect process temperature. According to the SEM images, it was formed that one film had one film thickness. As a result, it was found that the fabricated film was homogeneous and uniform. The thickness film was caused by the film at 500°C. The grain size and film thickness derived from SEM images were shown in table (2).

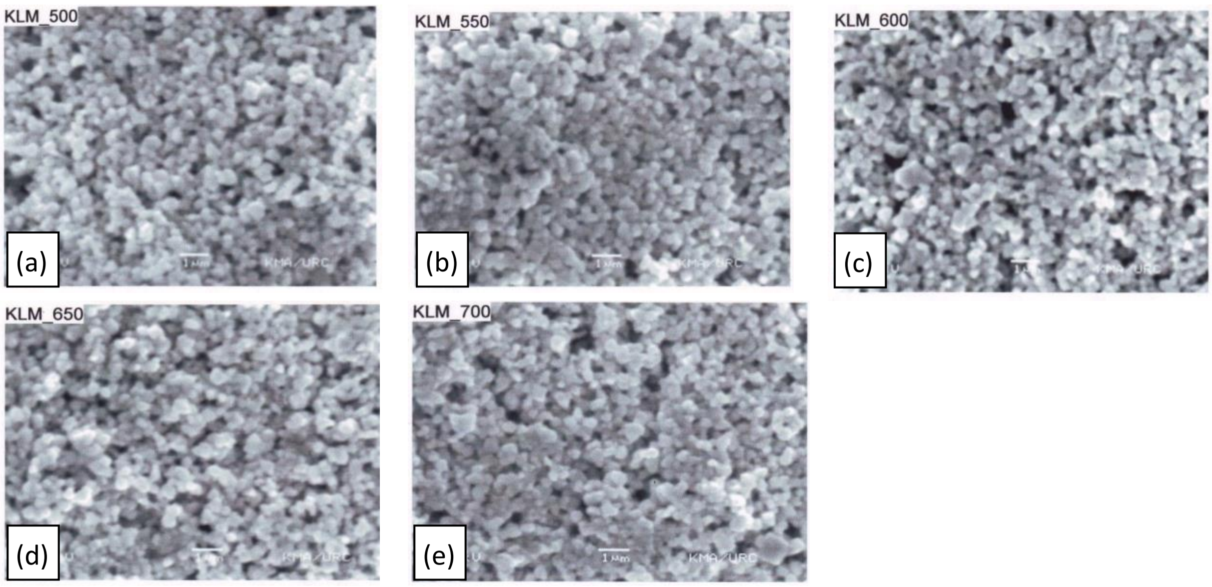

Figure (3). Surface morphology of SEM image of PCT/Si; (a). 500º C, (b). 550º C, (c) 600º C, (d). 650º C and (e) 700º C

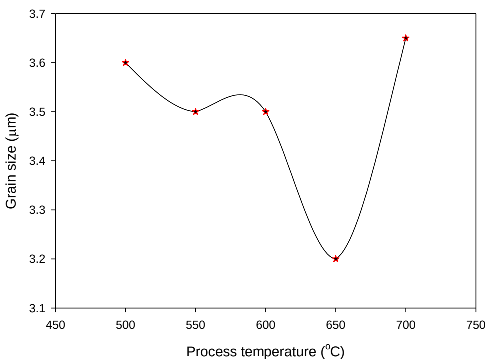

Figure (4). Change in grain size as a different process temperature

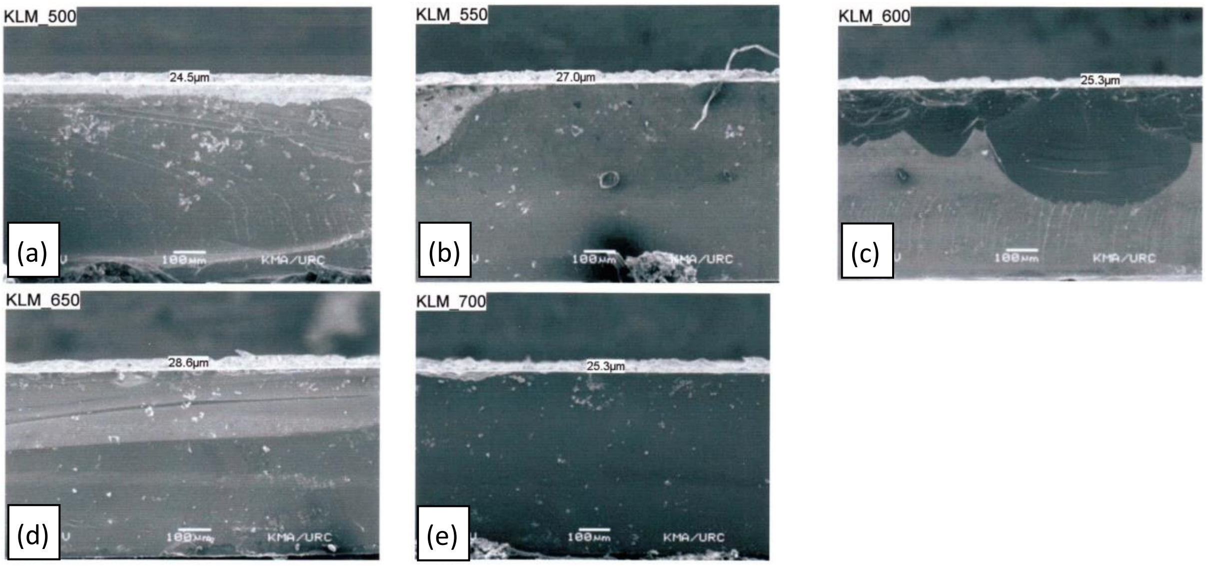

Figure (5). Scanning electron micrograph of cross section of film of PCT heated at; (a). 500º C, (b). 550º C, (c) 600º C, (d). 650º C and (e) 700º C

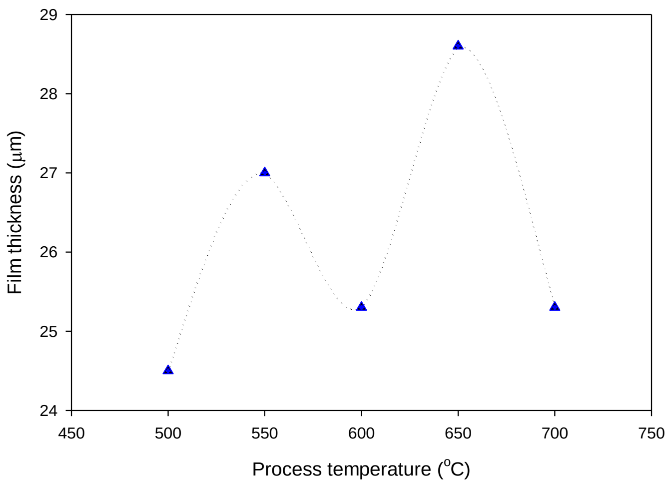

Figure (6). Film thickness as a function of process temperature

Table(2). Grain size and film thickness derived from SEM images

Temperature (°C)	Grain Size (µm)	Film thickness (µm)
500	0.36	24.5
550	0.35	27.0
600	0.35	25.3
650	0.32	28.6
700	0.37	25.3

In this paper, the voltage applied to gate electrode was defined as positive for the substrate to perform on the accumulation region so that there was no depletion in the substrate. In this measurement, moreover, the current flow was performed with the step voltage, 0.2 V and delay time, 1 min to avoid transient response.

As it can be seen in (Fig. 7.a), all I-V curves were similar. The current through the Cu/PCT/P-Si (100) cell increased exponentially with increase in voltage-drop across the fabricated cell in forward region. These curves showed the rectification effect. At the reverse region, it was found that, small amount of electrons flowed.

In clarify; asymmetric I-V curve was appeared as two distinct states such as I-V and I-V^2. The current was linearly increased at the low voltage region and exponentially rose at high voltage region. Thus, they also had properties or characteristics that enable them to perform many different electronic functions.

The low voltage resistance was measured from the linear part of forward region. The values were examined to 0.01 MΩ, 0.02 MΩ, 0.01 MΩ, 0.01MΩ and 0.01 MΩ, respectively. The width of dead-space could be estimated on forward part of I-V tracing. These values were 1.01 V, 1.52V, 1.02V, 1.52V, 1.53V, respectively. The maximum current flow was also observed. These values were also listed in table (3).

Table (3). V_{TH}, R and I_{max} at different process temperatures

Process temp (°C)	**500**	**550**	**600**	**650**	**700**
V_{TH} (V)	1.01	1.52	1.02	1.52	1.53
R (MΩ)	0.01	0.02	0.01	0.01	0.01
I_{max} (μA)	74	96	108	124	132

The purpose of this portion was concerned with the In I-V characteristics for the fabricated cell and to present it in graphical form to enable extraction of important diode properties such as η and ϕ_{bo}. The In I-V plot was represented as (Fig. 7.b). Appropriate linear functions were fitted to the curve and from the defined plot, the diode properties I_s and slope were formed. All I-V graphs obeyed the linear relationship and Is was obtained by extrapolating the variation line in which I_s=exp (intercept) relation was used. For calculation of diode parameters, equation 1 is used.

Using equation (1) , the value of the ideality factor η of diode at different temperature were calculated from the $\frac{\partial \phi bo}{\partial VF}$ in which V_F was limited 0 to 10 V in forward region since zero-bias barrier height, ϕ_{bo} has been determined from the experimental saturation current, I_s using equation (2). The resulting values were listed in table (4).

Table (4). η and ϕ_{bo} of the cell at different process temperatures

Process temp (°C)	**500**	**550**	**600**	**650**	**700**
η	1.41	1.37	1.38	1.34	1.32
ϕ_{bo}(eV)	0.29	0.27	0.27	0.26	0.24

Figure (7.c) gave the logI-logV plot at different process temperatures. Two different states were formed on logI-logV curve. The slopes of first states were examined to be about unity while those of second states were greater than 2. This indicated the well- defined transition voltage of fabricated films. (Fig. 7.d) shows the temperature dependence of ideality factor of PCT film. Variation of process temperature with zero-bias barrier height is depicted in (Fig. 7.e).

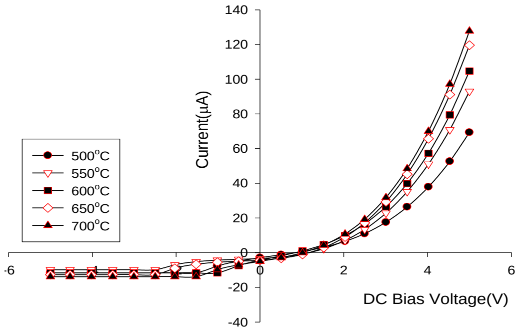

Figure (5). (a) Current and Voltage characteristics of PCT gated FMD with Cu-contact

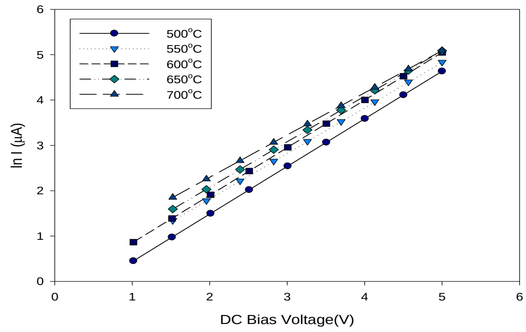

Figure (5). (b) Ln I-V characteristics of PCT gated FMD with Cu-contact

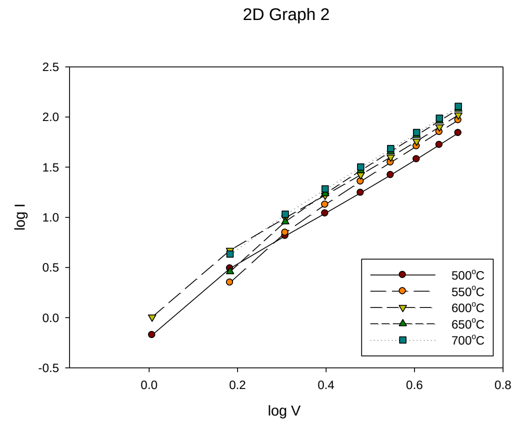

Figure (5). (c) logI-logV plot at different process temperature

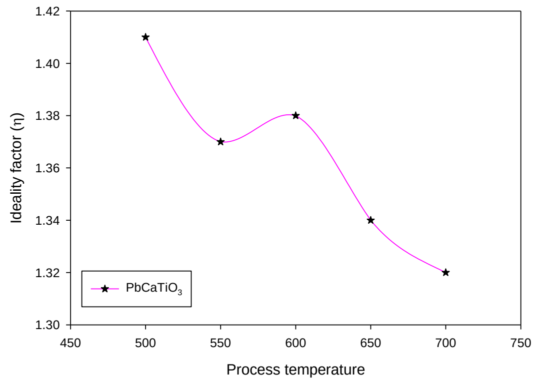

Figure (5). (d) Process temperature dependence of the ideality factor of PCT thin film

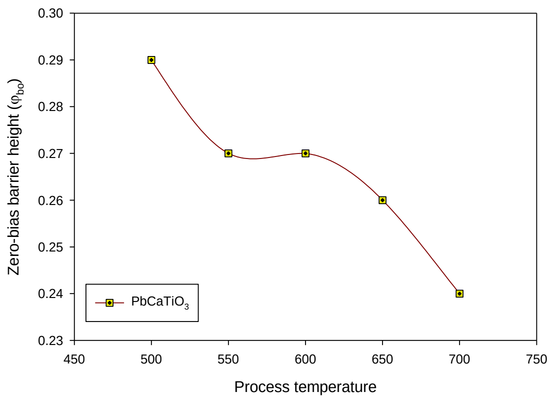

Figure (5). (e) Process temperature dependence of the zero-bias barrier height of PCT thin film

Conclusion

Fabrication and characterization of $Pb_{1-x}(Ca)_x TiO_3$ (x = 0.12 mol%) thin film have been carried out at different process temperature. From SEM microphotograph, it was found that the $Pb_{1-x}(Ca)_xTiO_3$ film was formed on Si-substrate with fine grain. According to the film thickness value, the film was said to be "thin film". All I-V curves were similar in variation nature. The current-flow through the Cu/PCT/P-Si (100) cell was exponentially increased with an increase in voltage-drop across the fabricated cell in forward region. These curves showed the rectification effect. At the reverse region, it was found that, small amount of electrons flowed. From this investigation, all ideality factor values were greater than unity. All calculated zero-bias barrier heights were found to be less than unity. I-V variation gave the nature of formation of Schottky barrier height. According to the above experimental results, the fabricated PCT film is quite suitable for non-volatile memory device application.

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